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Claims

[c1] A method of forming a strained Si/SGOI structure comprising the steps of:
providing a structure including a silicon germanium-on-insulator (SGOI) substrate, a strained Si layer atop the SGOI substrate, a gate dielectric atop the strained Si layer, a gate polySi atop the gate dielectric and a pad nitride atop the gate dielectric;
forming a first stack of said pad nitride, said gate polySi, said gate dielectric, said strained Si, and a relaxed SiGe layer of the SGOI substrate;
forming a trench oxide in regions adjacent to said first stack;
removing said pad nitride from said first stack to expose said gate polySi layer;
forming a material layer comprising a polySi layer, an insulator and a cap nitride on said exposed gate polySi layer and said trench oxide, said polySi layer is in contact with said gate polySi layer;
forming a second stack comprising said cap nitride, said insulator, said polySi layer, and said gate polySi layer, said second stack is located atop said gate dielectric; and

forming a raised source/drain region on said strained Si layer in regions adjacent to said second stack, wherein during said forming exposed sidewalls of the trench oxide are protected with a sacrificial nitride spacer.

[c2] The method of Claim 1 wherein SGOI substrate is formed by a process comprising thermally growing a SiGe layer atop a silicon-on-insulator layer and then relaxing the SiGe layer by annealing/oxidation; wafer bonding; wafer bonding and oxygen ion implantation; oxygen ion implantation into a SiGe wafer; providing a Si-containing substrate having a hole-rich region and a Ge layer, converting the hole rich region into a porous region, and annealing so as to convert the porous region into a buried oxide, while simultaneously forming a relaxed SiGe layer atop the buried oxide; or by thermal mixing.

[c3] The method of Claim 1 wherein said providing said first stack includes lithography and etching.

[c4] The method of Claim 1 wherein said trench oxide is deposited in said regions adjacent to said first stack, said deposited occurs in a single step or in multiple steps.

[c5] The method of Claim 1 wherein prior to forming said material stack said pad nitride is removed from the structure.

[c6] The method of Claim 1 wherein said forming said second stack comprises lithography and etching.

[c7] The method of Claim 1 wherein said forming said raised source/drain region comprises selective epitaxial Si growth.

[c8] The method of Claim 1 wherein said sacrificial nitride spacers are formed prior to forming said raised source/drain region by deposition and etching.

[c9] The method of Claim 1 further comprising removing said sacrificial nitride spacers to form divot regions on said strained Si layer, filling said divot regions with a nitride fill material, and forming oxide spacers on exposed sidewalls of said second stack.

[c10] A strained Si/SGOI structure comprising:
an active device region comprising a relaxed SiGe layer, a strained Si layer located atop the relaxed SiGe layer, a raised source/drain region located atop a portion of said strained Si layer, and a stack comprising at least a gate dielectric and a gate polySi located on another portion of the strained Si layer; and
a raised trench oxide region surrounding said active device region.

[c11] The strained Si/SGOI structure of Claim 10 wherein said relaxed SiGe layer is recessed as compared to the overlying strained Si layer.

[c12] The strained Si/SGOI structure of Claim 11 wherein said recess is not filled with any material.

[c13] The strained Si/SGOI structure of Claim 10 further comprising an oxide spacer abutting said stack.

[c14] The strained Si/SGOI structure of Claim 10 wherein said raised source/drain region is separated from said stack and said raised trench oxide by nitride.

[c15] The strained Si/SGOI structure of Claim 10 wherein said strained Si layer is in contact with said raised trench oxide region.

[c16] The strained Si/SGOI structure of Claim 10 wherein said gate polySi includes two polySi layers.

[c17] The strained Si/SGOI structure of Claim 10 wherein said gate dielectric is an oxide or an oxide containing nitrogen therein.

[c18] The strained Si/SGOI structure of Claim 10 wherein said gate dielectric is a thermal SiO_2 layer.

[c19] The strained Si/SGOI structure of Claim 10 wherein said

relaxed SiGe layer is an upper layer of a SGOI substrate, which further includes an underlying insulating layer, said insulating layer having said raised trench oxide region located thereon.

[c20] The strained Si/SGOI structure of Claim 10 wherein an oxide cap is present on said gate polySi.